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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,251	10/22/2003	Robert Haynes Isham	50190 (SE1928IP)	5456
7590	12/28/2004			EXAMINER BERHANE, ADOLF D
CHARLES E. WANDS, ESQ. ALLEN, DYER, DOPPELT, MILBRATH & GILCHRIST, P.A. 255 SOUTH ORANGE AVENUE, SUITE 1401 P.O. BOX 3791 ORLANDO, FL 32802-3791			ART UNIT 2838	PAPER NUMBER
DATE MAILED: 12/28/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/691,251	ISHAM, ROBERT HAYNES	
	Examiner	Art Unit	
	Adolf Berhane	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

**A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM
 THE MAILING DATE OF THIS COMMUNICATION.**

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on ____.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) Claim(s) ____ is/are allowed.
- 6) Claim(s) 1-12 is/are rejected.
- 7) Claim(s) ____ is/are objected to.
- 8) Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on ____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. ____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. ____. |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>2/20/04 & 6/5/04</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by

Dequina et al. (2004/0124818).

Dequina et al. disclose a mechanism for providing over-voltage protection during power up of DC-DC converter in Fig. 1. Electrical power for an integrated circuit (IC), such as but not limited to a microprocessor chip of a personal computer, is typically supplied by one or more direct current (battery) power sources, such as a buck-mode, pulse width modulation (PWM) based, DC-DC converter of the type diagrammatically shown in FIG. 1. As shown therein, a PWM control circuit (1) supplies a synchronous PWM signal to a switching circuit driver (2) that controls the turn-on and turn-off of a pair of electronic power switching devices (3 and 4), to which a powered load (9) is coupled. In the illustrated DC-DC converter, the electronic power switching devices comprise an upper (or high side) power NMOSFET (or NFET) device (3), and a lower (or low side) power NFET device (4), having their drain-source current flow paths connected in series between a pair of power supply rails (e.g., VIN and ground (GND)).

The upper NFET device (3) is turned on and off by an upper gate-switching signal UGATE applied to its gate from driver (2), while the lower NFET device (4) is turned on and off by a lower gate-switching signal LGATE supplied from driver 92). A common or phase node (5) between the two NFETs is coupled through an inductor (6) to a load reservoir capacitor (7) that is coupled to a reference voltage terminal (GND). The connection (8) between inductor (6) and capacitor (7) serves as an output node from which a desired (regulated) DC output voltage Vout is applied to a LOAD (9) (coupled to GND).

The output node connection (8) is also fed back via a feedback resistor (10) to error amplifier circuitry within the PWM controller (1). The error amplifier circuitry is used to regulate the converter's DC output voltage relative to a reference voltage supply. In addition, the common node (5) between the controllably switched NFETs is coupled via a current sense resistor (11) to current-sensing circuitry within the controller (1), in response to which the controller adjusts duty ratio of the PWM signal, as necessary, to maintain the converter's DC output within a prescribed set of parameters.

In the course of supplying power from the power supply to its powered components, it is of critical importance that an anomaly in the power supply path, such as a short circuit in the upper switched NFET (which may be due to a bad component or inadvertent shorting of its drain and during manufacture), not propagate to downstream circuitry, especially a microprocessor chip.

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Thereby providing through the lower device (4) a bypass for an overvoltage that would otherwise be coupled from the regulated voltage output terminal to the load.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Saeki et al disclose a DC-DC converter capable of preventing overvoltage.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adolf Berhane whose telephone number is 571-272-2077. The examiner can normally be reached on Monday- Friday 8 AM to 6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Adolf Berhane
Primary Examiner
Art Unit 2838